REMARKS/ARGUMENTS

Applicants wish to thank Examiner for the reading of their response to the previous office action of 6/14/2005. As we have stated previously, the present claimed invention is novel over prior art double resonant tunneling diodes in that its double dielectric tunneling barrier layers are formed of particular dielectric materials that have a low band offset relative to the conduction band edge of the semiconductor material forming the quantum well. The use of these materials have been shown by the applicants to significantly improve the performance of the device. Thus, if the quantum well is formed, for example, of silicon or germanium, the dielectric material can be Si_3N_4, HfO_2, ZrO_2, Y_2O_3, Pr_2O_3, TiO_2, Al_2O_3, or Ta_2O_5, or their alloys or laminates, as in claim 4. Prior art resonant tunneling diodes have used other materials as barrier layers, but it is found herein that the combination of these low band offset materials and the silicon or germanium well materials produces a device of particularly good performance as noted in the application.

Before responding to Examiner's present rejections, applicants would like to first respectfully address Examiner's responses to applicant's previous arguments as Examiner has set them forth beginning on page 6 of the present paper.

Examiner states that: "Krivokapic teaches a tunneling barrier layer being formed of a dielectric material characterized by a low band offset relative to the conduction band edge of said semiconductor material." Yet, in referring to his Fig. 5, Krivokapic clearly states (column 4, lines 3-5): "thin portions of undoped silicon **208** lay between the n+ doped region **204** and the p+ doped regions **206** and serve as tunneling barriers between

n+ doped regions **204** and the p+ doped regions **206**." Thus, in Krivikapic's invention the tunneling barrier layers are not the low band offset dielectric layers of the present claimed invention but are undoped regions of Si semiconductor material. Moreover, in the present claimed invention, there is a single layer of low band offset dielectric material on either side of the Si quantum well, forming, thereby, a single, double barrier resonant diode. Krivokapic, on the other hand, forms two Si barriers within a pair of diodes in series, to form a latch. Thus, each of Krivokapic's diodes includes only a single barrier layer and is not a double barrier resonant diode in the sense of the present claimed invention. Krivokapic's invention is pictured in his Fig. 5 as a p+ region (206), a first Si barrier layer (208), an n+ region (204), a second Si barrier layer (208) and a second p+ region (206). This symmetric superposition of five regions comprises a latch (two diodes in series) not the single resonant tunneling barrier layer of the present claimed invention. Inspection of Krivokapic's Fig. 3 discloses the basic form of the resonant tunnel diode that Krivokapic is forming, in a back-to-back configuration to complete his latch. The tunnel diode of Fig. 3 includes a single barrier and is unlike the double barrier diode of the present claimed invention. Although Krivokapic denotes Fig. 3 as "prior art," it is prior art only in the sense that his invention is fabricated differently and includes two of the diodes of Fig. 3 in series.

Examiner argues further that: "Figure 5 of Krivokapic clearly depicts undoped regions 208 (sic) abutting the vertical layer 208" (applicant believes that Examiner is referring to undoped regions that are not numbered and that are above the buried oxide layer (210) and beneath the latch structure). These undoped regions have nothing to do

with Krivokapic's invention, however, and are simply regions that lie below the doped regions 204 and 206.

Examiner also argues that: "Claim 10 recites an SOI substrate. Krivokapic teaches an SOI substrate. Therefore, Krivokapic's structure is identical to the claimed structure, even if the SOI substrate is used differently by Krivokapic and by the present applicants." Krivokapic's invention is formed by implanting ions within an SOI substrate through a dummy masking gate on the substrate surface to create regions 204, 206 and 208. In fact, Krivokapic's Si barrier layer is a region that is blocked from the injected ions by the masking gate on the upper surface of his substrate. Krivokapic states (column 3, lines 42-44): "Additionally, the dummy gate serves as a masking agent thereby preventing the masked area from being doped by the first ion implant." The present claimed invention is formed on the upper surface of a SOI substrate, it is not formed by the implantation of ions into regions that are interior to the SOI substrate. Applicants would now respectfully respond to the claim rejections in the present paper.

Claim Rejections- 35 USC 102/3

Applicants respectfully request reconsideration of the rejection of claims 1, 3 and 10 as being anticipated by or, in the alternative, obvious over Krivokapic (US Patent No. 6,291,832) for the following reasons.

Krivokapic teaches the formation of a resonant tunneling diode latch, which is two resonant tunneling diodes in series formed by ion-implantation within a SOI substrate. As illustrated in Krivokapic's Fig. 5 and according to his description in lines

3-6 of column 4, the "thin portions of undoped silicon 208 lay between the n+ doped region 204 and the p+ doped regions 206 and serve as tunneling barriers". Krivokapic uses the same language in his claim 1, namely in lines 11 and 12, "...the tunneling barrier being an undoped portion of the silicon substrate." Comparing Krivokapic's Fig. 3 with his Fig. 5, it can be seen that his latch is formed by the back-to-back integration of two of the Fig. 3 diodes.

In the language of the present claimed invention, as recited in claim 1, the claimed barrier layers are the low band offset dielectric layers formed on either side of the quantum well, providing a potential barrier to injected electrons. Krivokapic does not have such low band offset dielectric barriers in his invention. Krivokapic's barrier layer is a layer of undoped Si. Applicants would, therefore, argue that neither of diodes in the series configuration of Krivokapic is a double barrier resonant diode as is claimed in the present application because Krivokapic's series configuration does not have low band offset dielectric barrier layers disposed against the sides of a quantum well layer. This can be seen in Krivokapic's Fig. 5. In addition to the lack of the low band offset dielectric barrier layers, Krivokapic's invention differs in yet another significant way from the present claimed invention, in that it is a latch, series combination of two diodes, neither of which is the diode of the present claimed invention. In column 2, lines 65-67, continued in column 3, lines 1-4, Krivokapic states: "A latch, for the purposes of this patent application, comprises two diodes in series. Accordingly, the method and system in accordance with the present invention allows for the creation of two resonant tunneling diodes in series..." In Krivokapic's device, as illustrated in his Fig. 5, there are two diodes formed in a back-to-back configuration. One diode is p^+ Si to undoped Si to n^+ Si

(shown as regions 206, 208 and 204 in Fig. 5), the second diode is the same n^+ Si to undoped Si to p^+ Si, (shown as regions 204, 208 and 206 in Fig. 5). Thus, layer 204 serves as a part of a diode in each of the two series diodes. This construction is discussed in column 3, lines 63-68 and column 4, lines 1-6 of Krivokapic. In the present claimed invention, there is only one diode and any similarities between Fig. 7 of the present Application and Fig. 5 of Krivokapic are purely superficial. In applicant's Fig. 7, the diode is formed on the upper surface of a SOI substrate. In Krivokapic's Fig. 5, the diode latch is formed within the interior of a SOI substrate. The present claimed diode can, therefore, utilize a quantum well layer of other semiconductor material, whereas Krivokapic is limited to the material forming the interior of a SOI substrate. The operational principles of Krivokapic's back-to-back diodes and the present claimed diode with low band offset barrier layers are completely different. Examiner notes that: "the claimed limitations of a quantum well layer formed by photolithographic patterning and etching and a tunneling barrier layer formed by a process of CVD, ALD or sputtering are process limitations which would not carry patentable weight in this claim drawn to a structure." Amended claim 1 now recites the limitation (described in the specification and illustrated in Fig. 7) that the diode is formed on the horizontal surface of the substrate and applicants would respectfully argue that this is a patentable difference between their claimed invention and that of Krivokapic. Further, this quantum well, having parallel, planar vertical sides (line 8 of present claim 1), is not any layer of the invention described or claimed by Krivokapic. Similarly, in the present claimed invention the dielectric barrier layers formed of low band offset material are formed by a deposition process of

CVD, atomic layer deposition or sputtering on the vertical sides of the quantum well. Such barrier layers are neither formed nor do they exist in the invention of Krivokapic.

For the reasons described above, Applicants respectfully argue that their claims 1 and 3 are not anticipated by the invention of Krivokapic. Similarly, Applicants respectfully argue that their claim 10, goes well beyond any description or claims of Krivokapic. While Krivokapic does form his latch configuration within a SOI substrate, his configuration is formed by a doping process that defines his barrier layer as being a region that is masked from the injected ions. In the present claimed invention, the upper surface of a SOI substrate is used to create the quantum well layer through a photolithographic etching process and the dielectric layers are not formed from the SOI substrate material, but are formed of low band offset materials on the well layer by various deposition processes using material not taken from the SOI substrate. For example, this fabrication method is compatible with the technology of CMOS FinFet structures, which is highly desirable. Thus, the SOI substrate is used differently by Krivokapic and the present applicants. Moreover, although an SOI substrate is used by both Krivokapic and the present applicants, the final configuration formed thereon is patentably different. Therefore, the present applicants respectfully argue that they can claim (in claim 10) the use of the SOI substrate with which to form their invention and not be anticipated by Krivokapic.

Claim Rejections- 35 USC §103

Applicants respectfully request reconsideration of the rejection of claims 2 and 4-9 as being unpatentable over Krivokapic for the following reasons. Examiner argues that

Krivokapic teaches substantially the entire claimed structure of the present application. Applicants would respectfully point to their previous argument in which they have shown that the invention of Krivokapic is distinct from the present claimed invention. Applicants would argue, in particular, that one skilled in the art would find no place in Krivokapic's invention to form low band offset dielectric layers. Since the barrier layer of Krivokapic is formed internally as a region of the SOI substrate that is undoped, it could not be replaced by low band offset layers.

Claim 2 of the present claimed invention claims a quantum well layer of Si, Ge or SiGe. As discussed above, the layer claimed in the present invention is not the same as any layer claimed by Krivokapic. Examiner suggests that it would be obvious to a person of ordinary skill in the art to use other semiconductor material for the quantum well. While this might be obvious, it would also be impossible. Since the quantum well in Krivokapic is a doped region within the SOI substrate, this region could not be replaced by other semiconductor material.

Regarding claim 4, Examiner asserts that it would be obvious to a person of ordinary skill to use the low band offset dielectric material of the present claimed invention. Since the barrier layer of Krivokapic is an undoped region within a SOI substrate, it would be impossible to replace this region by any other dielectric material. It is the entire essence of Krivokapic's invention that an integral two-diode structure can be formed by masking an SOI substrate so that an undoped barrier layer is formed as a result of injecting ions to form other portions of the diode system. Since a substantial portion of Krivokapic's novelty resides in this manner of forming a barrier layer, why would one of ordinary skill following the teachings of Krivokapic find a suggestion to form a barrier

layer of other dielectric material? For the same reason, applicants respectfully suggest that claims 5, 7 and 8, reciting the dimensional limitations of the well and barrier layers, are not suggested by the teachings of Krivokapic.

If the Examiner has any questions regarding the above application, please call the undersigned attorney at 845-452-5863

Respectfully submitted,

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